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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,654	CHEN ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14 and 16-19* is/are rejected.

7)☒ Claim(s) *7,15 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Drawing

The amendment and drawing submitted on Apr 4, 2005 were reviewed and considered with the following results:

The replacement sheet overcame the objection to Fig. 5, which has now been withdrawn.

The amended paragraphs overcame their respective objection described in the previous Office Action. Therefore, those objections have also been withdrawn.

Although the amended claims overcame all the rejections of claims 4-7, 12-15, and 19-20 under 35 U.S.C. 112, as described in the previous Office Action, the amended change to claim 4 created a new concern. This is described later under the Objections to Claims' section, while the previous Office Action's rejections under 35 U.S.C. 112 have all been withdrawn.

The rejections of claims 1-6, 8-14, and 16-19 under 35 U.S.C. 102(b), with respect to Takeyabu et al., have been basically maintained. These rejections are described later under the appropriate section, with slight modifications to better clarify the examiner's interpretation of the claim limitations with respect to the prior art reference, and the applicants' arguments/comments. Related comments are described under the Response to Arguments section.

Claim Objections

Claims 4-7 are objected to because of the following informality: The phrase "greating restriction" is confusing in claim 4, but it is believed the phrase was meant to be "greatly restricting" as corresponding amended claims 12 and 19 now recite. Claims 5-7 carry over the objection from claim 4. Therefore, an appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-14, and 16-19 remain rejected under 35 U.S.C. 102(b) as being anticipated by Takeyabu et al. (Takeyabu), a reference cited in the previous Office Action. Fig. 16 shows a circuit, that can be labeled as a high-speed low-noise charge pump, comprising first cascode current mirror NT11-NT13,NT15 coupled to first reference current source 121 and adapted to generate a first mirror current (unlabeled but understood as being applied to the output node between PT15 and NT13 when the first cascode current mirror's output current flows), wherein the first cascode current mirror includes first output mirror transistor NT15 and first output cascode transistor NT13; second cascode current mirror PT11-PT13,PT15 coupled to second reference current source NT16-NT17 and adapted to generate a second mirror current (unlabeled but understood as being applied to the output node when the second cascode current mirror's output current flows), wherein the second cascode current mirror includes second output mirror transistor PT13, and second output cascode transistor PT15 coupled to first output cascode transistor NT13 at the output node; first switching transistor NT14 being turned on during assertion of a first control signal (output Q of 126 is high) to cause the first mirror current to flow; and second switching transistor PT14 being turned on during assertion of second control signal (output Q of 126 is low) to cause the second mirror current to flow. Since the source, drain, and gate of first switching transistor NT14 are coupled to first output mirror transistor

NT15, first output cascode transistor NT13, and to receive the first control signal, respectively, and the source, drain, and gate of second switching transistor PT14 are coupled to second output mirror transistor PT13, second output cascode transistor PT15, and to receive the second control signal, respectively, claim 1 is anticipated. NT13-NT15 are n-channel MOS transistors, and PT13-PT15 are p-channel MOS transistors, thus anticipating claim 2. The source and drain connections of transistors NT13-NT15, and PT13-PT15 are clearly shown in Fig. 16, and understood by one of ordinary skill in the art. Therefore, claim 3 is also anticipated. The combination of the first/second cascode current mirrors is deemed a wide swing cascode current mirror because they allow the voltage provided at the output node to substantially range between the (positive) voltage supply and the (low) voltage supply (e.g. ground), anticipating claim 4 for the following reasons: 1) When PT14 is off and NT13 is on, PT14 provides a high impedance between the output node and the positive voltage supply. This prevents, or minimizes, any leakage current of the second cascade current from flowing to the output node through PT13-PT15 that would pull the output voltage to a slightly higher level. Therefore, without this leakage current, conduction of NT13-NT15 allows the output voltage to be pulled as low as possible (with respect to any voltage drop across NT13-NT15). 2) With similar type reasoning, when PT14 is on and NT13 is off, NT13 provides a high impedance between the output node and the low voltage supply (e.g. ground), and the output voltage is effectively pulled high (with respect to any voltage drop across PT13-PT15). The first cascode current mirror further comprises first input mirror transistor NT12 coupled to first output mirror transistor NT15 and ground, and first input cascode transistor NT11 coupled to first output cascode transistor NT13 and first reference current source 121; and the second cascode current mirror further comprises

second input mirror PT11 coupled to second output mirror transistor PT13 and the voltage supply, and second input cascode transistor PT12 coupled to second output cascode transistor PT15 and second reference current source NT16-NT17 to anticipate claim 5. NT11-NT12 are n-channel MOS transistors, and PT11-PT12 are p-channel MOS transistors, anticipating claim 6. Interpreting Fig. 16 in a slightly different manner, reference current source 121 provides a supply current directly to first cascode current mirror NT11-NT13,NT15, and effectively (e.g. indirectly) provides the supply current to second cascode current mirror PT11-PT13,PT15. Therefore, reference current source 121 is considered as being coupled to the first/second cascode current mirrors, and claims 8-14 are anticipated for the same type of reasoning as applied to claims 1-6 as previously described. With similar reasoning, but in yet another interpretation of Fig. 16, first switching transistor NT14 has its source, drain, and gate coupled to the drain of first output mirror transistor NT15, the source of first output cascode transistor NT13, and to the first control signal, respectively, and second switching transistor PT14 receives a second control signal to cause the second mirror current from second cascode current mirror PT11-PT13,PT15 to flow. Since NT13 and NT15 are included within first cascode current mirror NT11-NT13,NT15, claims 16-19 are anticipated for the same reasoning as applied to previous, corresponding claims (e.g. see claims 3-4).

No claim is allowable, as presently written.

Allowable Subject Matter

However, claims 7, 15, and 20 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation

to modify or combine any prior art reference to ensure the drain of the input cascode transistor is coupled to the gate of the corresponding input mirror transistor as recited within claims 7 (lines 4-5 and 9-10), 15 (lines 4-5 and 9-11), and 20 (lines 5-6).

Prior Art

The prior art reference cited on the accompanying PTO-892 is deemed relevant to the claimed invention. Prior Art Fig. 2 of Svärd shows first cascode current mirror N7-N10 coupled to first reference current source P2,P5; second cascode current mirror P1,P3,P4,P6 coupled to second reference current source IREF; first switch S4 coupled between first output mirror transistor N10 and first output cascade transistor N8, wherein first switch S4 is controlled by first control signal Down; and second switch S1 coupled between second output mirror transistor P3 and second output cascade transistor P6, wherein second switch S1 is controlled by second control signal Up. Although this reference does not clearly show or disclose the switches as being transistors controlled by a signal being applied to their respective gate, it would be obvious to one of ordinary skill in the art to replace Svärd's generic type switches S1-S4 with MOS transistors, to correspond to MOS transistors P1-P6 and N7-N10 already within the circuit. These transistors are well known means for providing a switching means, and the MOS switching transistors would provide similar operating characteristics as the other MOS transistors (e.g. with respect to temperature and voltages). Therefore, this reference should be carefully reviewed and considered.

Also, it is suggested that all of the other prior art references cited on the previous Office Action's PTO-892 be carefully reviewed and considered with respect to what those references actually show and disclose.

Response to Arguments

The applicants' arguments filed Apr 4, 2005 have been fully considered but they are not persuasive. The applicants argue that: 1) Takeyabu's signal Q would not be reasonably interpreted as first/second control signals; 2) the first/second control signals have four possible states; 3) the output current varies from a positive value, to zero, to a negative value; and 4) the claimed arrangement achieves a fast switching speed.

1) The applicants' arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The claims recite "assertion of a first control signal" and "assertion of a second control signal", or "the first control signal is asserted" and "the second control signal is asserted", without clearly identifying what can be considered a "control signal." Fig. 16 of Takeyabu shows flip-flop 126 providing signal output Q, which one of ordinary skill in the art would understand has two states (i.e. logic high and logic low). Using the broadest reasonable interpretation with respect to what can be considered a control signal, and/or first/second control signals, the following reasoning has been applied to Takeyabu's output signal Q and the applicants' recited first/second control signals. Deeming logic high as an asserted first control signal, it allows first switching transistor NT14 to turn on and current will then flow from the output node (between PT15 and NT13) to ground. When the logic level is low, the first control signal can be considered absent, and first switching transistor NT14 is off. However, the logic low level can be deemed an asserted second control signal with respect to the signal that allows second switching transistor PT14 to turn on and current to flow from the positive voltage supply to output node (between PT15 and NT13).

The asserted second control signal is considered absent when the signal is at logic high, and therefore second switching transistor PT14 is off.

2-4) In response to the other arguments/comments by the applicants that imply the Takeyabu reference fails to show certain features of the applicants' invention, it is noted that the features upon which the applicants rely (i.e., the first/second control signals have four possible states; the output current varies from a positive value, to zero, to a negative value; and the claimed arrangement achieves a fast switching speed) are not clearly recited within the body of the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The following remarks will address each of the above arguments with respect to the examiner's broadest reasonable interpretation of the actual claimed limitations. One of ordinary skill in the art would understand a signal could have various states (e.g. logic high, logic low, high impedance, linear, non-linear, etc), and even if each control signal has only two states, a pair of control signals could be complementary to one another (i.e. one would be high when the other is low); or they could be in a phase shifted type relationship with one another, wherein during certain periodic durations of time, both signals could be high, both could be low, or one could be high while the other is low. Therefore, where in the recited limitations are the signals clearly identified as being distinct from one another, and they provide the four possible states cited on the amendment's page 13? Similarly, where in the claims is the zero value of the output current recited? Even if it was, one of ordinary skill in the art would understand Takeyabu's circuit provides positive, negative, and zero currents. For example, a positive current is provided to charge capacitor C10 when switching transistor PT14 is on (and

switching transistor NT14 is off) and current flows from the positive voltage supply to ground via PT13-PT15 and C10; a negative current is provided to discharge capacitor C10 when switching transistor NT14 is on (and switching transistor PT14 is off) and current flows from the capacitor to ground via NT13-NT15; and the current is at zero temporarily when the circuit transitions between the charging and discharging portions of the circuit's operation. With respect to the "fast switching speed", where is that clearly recited within the bulk of the claims, providing at least some weight to the "high-speed" label recited in the preamble?

Therefore, the rejections described in this Office Action, and the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of what is actually be claimed. As such, one of ordinary skill in the art would understand that the reference of Takeyabu et al. shows/discloses a "high-speed low-noise charge pump" as recited with the present application's rejected claims.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.L.E

Terry L. Englund

24 June 2005

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